ABSTRACT OF THE INVENTION

A memory system having a memory controller and several separate memory devices connected to the controller by a system bus. The memory devices each included an array of memory cells, addressing circuitry used to address the cells and an address storage circuit which stores a local address unique to each of the memory devices. The local addresses are sequentially assigned to the memory devices by selecting a first one of the devices and forwarding an address assign command to the selected device. A command decoder, having detected the address assign command, will permit a local address placed on the bus by the controller to be loaded into the selected memory device. This sequence will continue until all of the memory devices have been assigned local addresses at which time the memory devices can be accessed to perform memory read, program, erase and other operations.